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Announcement of Advanced High Resolution CD-SEM CG6300

- For development of 7 nm generation devices and mass production of 10 nm generation devices -

Tokyo, Japan, July 14, 2015 — Hitachi High-Technologies Corporation (TSE:8036, Hitachi High-Tech) announced today introduction of the latest model of its advanced high resolution CD-SEMs[*1], the CG6300.
Hitachi High-Tech launched its first CD-SEM in 1984. The units have won strong approval for their excellent repeatability and high resolution, and Hitachi High-Tech has grown to become the defacto standard in the field of metrology creating a market for electron-beam measurement and shipping over 4,600 units. The CG6300 represents a full model change from the existing CG5000, geared towards the latest process controls for development of 7 nm generation devices and mass production of 10 nm generation devices. It is scheduled for launch in October 2015.

Advanced device manufacturers begun to work on the development of 7 nm generation devices and the mass production of 10 nm generation devices. The mainstream methods for achieving these refinements are repeated LELELE[*2] processes using immersion lithography systems and SAQP[*3] multiple patterning[*4] using deposition and etching systems. Meanwhile, in FinFET[*5], 3D-NAND[*6] and DRAM[*7], the introduction of 3D and high-spec construction requires accurate measurement of the bottom dimension of deep trenches and holes. Advanced device manufacturers are also facing the issue of an increase in the numbers of masks and inspection processes associated with these refinements.

Advanced high resolution CD-SEM is a practical application of the scanning electron microscope that measures the dimensions of fine patterns of semiconductors formed on wafers.
The newly developed CG6300 will offer higher resolution with a fully renewed electron optical system along with improved metrology repeatability and image quality. The electron microscope column is able to select secondary electrons (SE[*8]) and backscattered electrons (BSE[*9]) emitted from the material depending on the measurement target. In this way, the system is able to measure the bottom dimensions of deep trenches and holes in via-in-trench[*10] BEOL process[*11] as well as 3D NAND and DRAM. Furthermore, a two-fold increase in the scanning speed of the electron beam compared to the existing model has reduced the effect of static electricity on the wafer surface, enabling a higher resolution image to be obtained and high-contrast edge detection. In addition, a newly designed stage will increase productivity with a 20% boost in speed in terms of the number of wafers processed per hour, thereby reducing the cost of ownership[*12] to the user.
Moreover to meet the needs of device mass production, matching between the systems will be improved to realize stable long term stability.

With the development of the CG6300, Hitachi High-Tech will provide high precision measurement functions for advanced devices to a wide range of users, and high-end users in particular.

*1 CD-SEM (Critical Dimension SEM): A scanning electron microscope (SEM) for measuring the microscopic circuit pattern on semiconductor wafers.

*2 LELELE (Litho–Etch–Litho–Etch–Litho–Etch): A method of refining photolithography and etching through repetition.

*3 SAQP (Self Align Quadruple Patterning): A miniaturization method in which side-wall deposition is performed twice. Refinements are made not only by the exposure, but also by the thickness of the sidewall layer.

*4 Multiple-patterning: A method of refinement using other processes in addition to exposure processes such as LELELE and SAQP.

*5 FinFET (Fin Field Effect Transistor): A field effect transistor with a 3D-type construction.
*6 3D-NAND: A 3D NAND flash memory.
*7 DRAM (Dynamic Random Access Memory)
*8 SE (Secondary Electron): An electron that is emitted from a material upon being irradiated by an electron beam.
*9 BSE (Back Scattering Electron): A beam electron that is reflected backward.
*10 Via-in-trench: A structure whereby a hole is provided at the bottom of a trench in the BEOL process, creating a higher aspect ratio than conventional structures.
*11 BEOL process (Back End Of Line): The wiring formation processes within the front-end processes of semiconductor manufacturing.
*12 Cost of Ownership: The total cost necessary for installation, operation and management of facilities, equipment, and other hardware.

Advanced High Resolution CD-SEM CG6300

Main Features

- High resolution enabling high precision measurement of 7 nm generation devices
- Improved visibility of deep trench and contact holes dimensions as well as material contrast
- High contrast imaging through selective performance enhancement of SE and BSE signals
- Clear, noise-free images using multiple scanning methods including high-speed scanning
- Wafer transport system featuring a newly designed high-speed stage

Main Specifications

Wafer size	Φ300 mm (SEMI standard V notched wafer)
Auto-loader	3 FOUP*13-compatible random access
Power supply	Single-phase AC200 V, 208 V, 230 V, 12 kVA (50/60 Hz)

*13 FOUP (Front-Opening Unified Pod): A standard front-opening cassette integrated transport and storage container used in semiconductor plants.

Contact
Yutaka Okagawa, Toru Ikegami
Process Control Systems Dept. 2,
Semiconductor Process Control Systems Div.,
Electronic Device Science Systems Business Group
Tel: +81-50-3139-4726

For Media Inquiries
Reiko Takeuchi, Shinji Ito
Corporate Communications Dept., CSR Div.,
Tel: +81-3-3504-7760